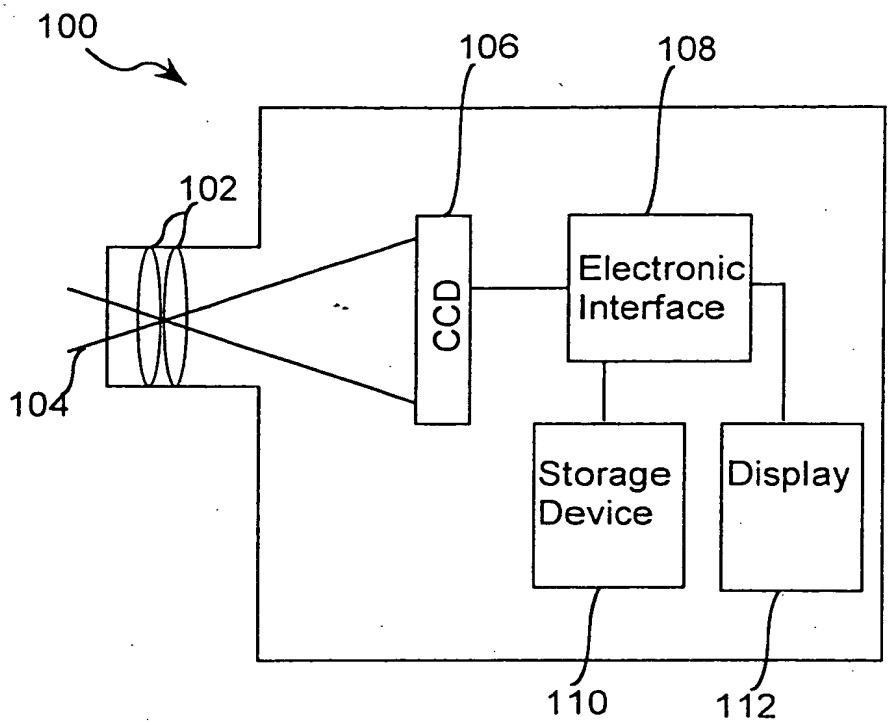

100
106
108
102
CCD
Electronic Interface
104
Storage Device
Display
110
112

FIG. 1

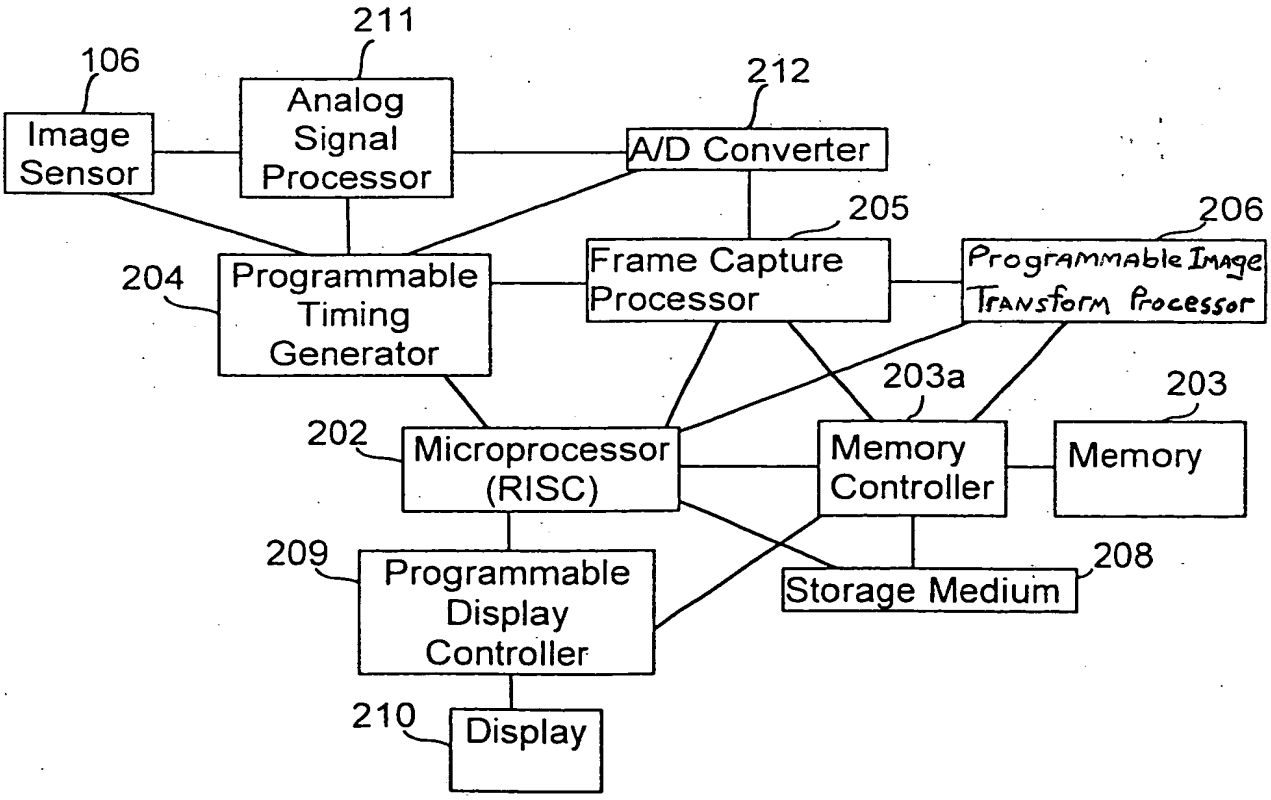

211
106
212
Analog Signal Processor
Image Sensor
A/D Converter
205
206
204
Programmable Timing Generator
Frame Capture Processor
Programmable Image Transform Processor
203a
203
202
Microprocessor (RISC)
Memory Controller
Memory
209
208
Programmable Display Controller
Storage Medium
210
Display

FIG. 2

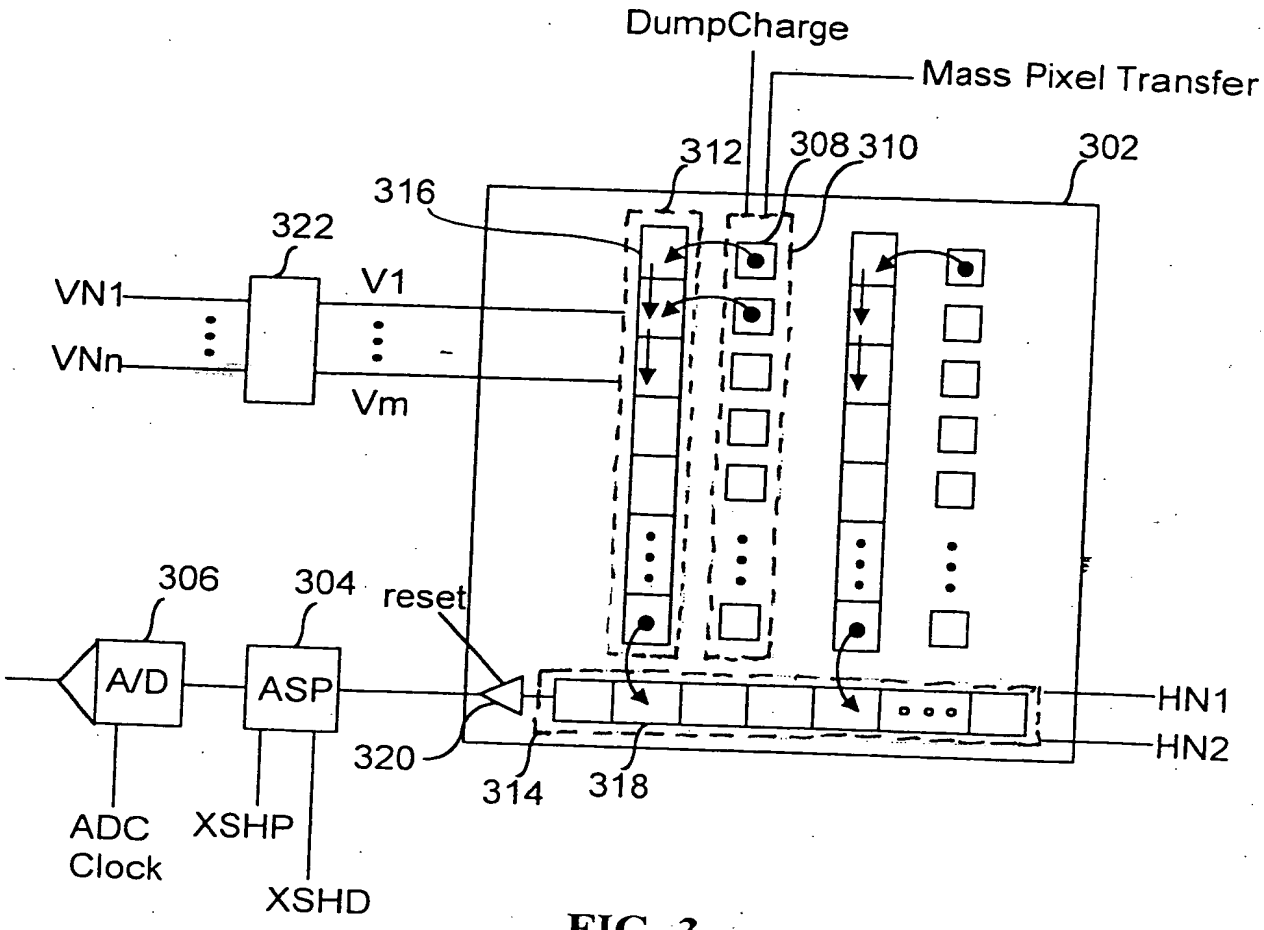

DumpCharge
Mass Pixel Transfer
312
308
310
302
316
322
VN1
VNn
V1
Vm
306
304
reset
A/D
ASP
320
314
318
HN1
HN2
ADC
Clock
XSHP
XSHD

FIG. 3

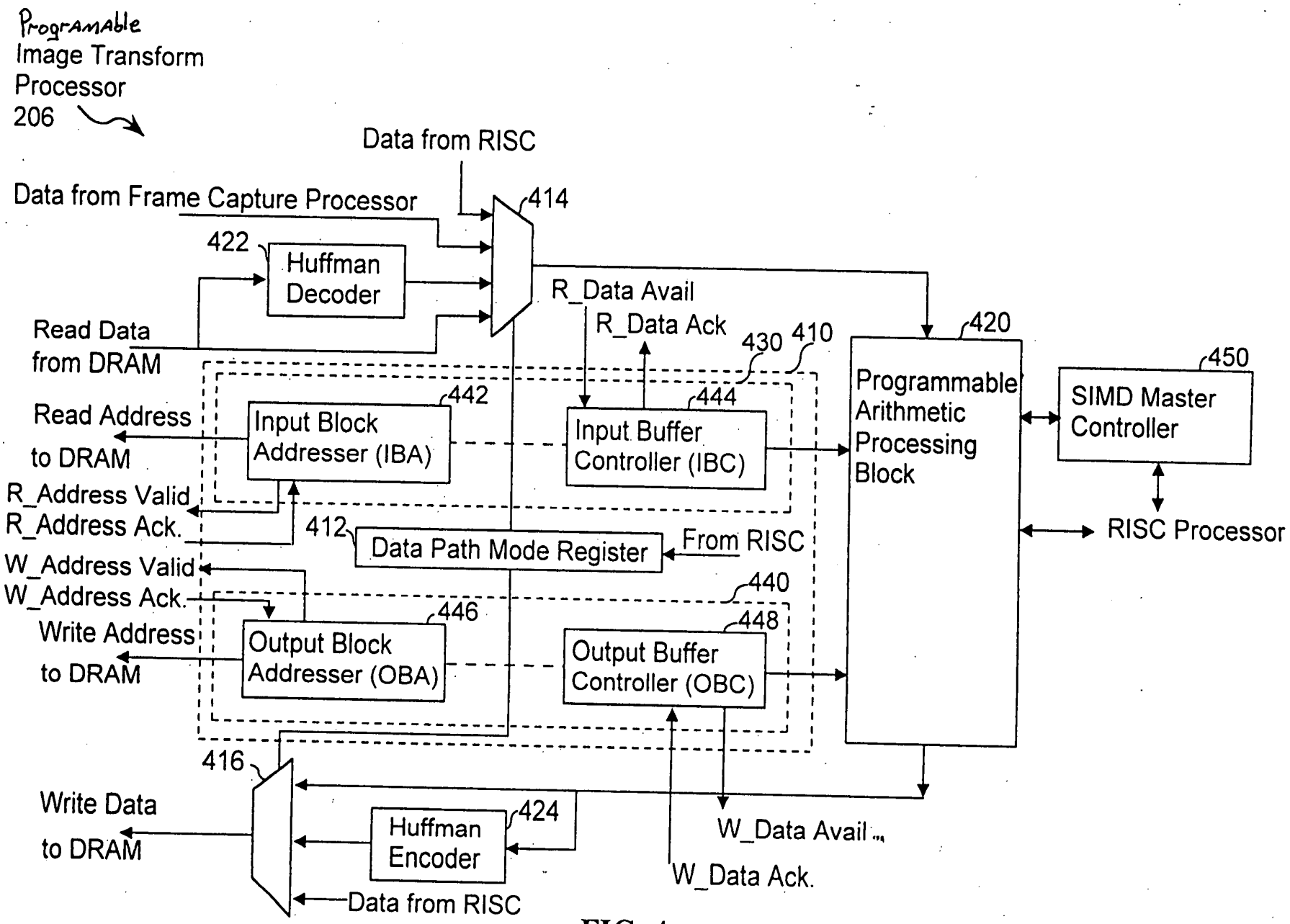

Programable
Image Transform
Processor
206
Data from RISC
Data from Frame Capture Processor
414
422
Huffman
Decoder
R_Data Avail
R_Data Ack
Read Data
from DRAM
430
410
420
450
Programmable
Arithmetic
Processing
Block
SIMD Master
Controller
442
444
Read Address
to DRAM
Input Block
Addresser (IBA)
Input Buffer
Controller (IBC)
R_Address Valid
R_Address Ack.
412
Data Path Mode Register
From RISC
RISC Processor
W_Address Valid
W_Address Ack.
440
446
448
Write Address
to DRAM
Output Block
Addresser (OBA)
Output Buffer
Controller (OBC)
416
Write Data
to DRAM
424
Huffman
Encoder
W_Data Avail
W_Data Ack.
Data from RISC

FIG. 4

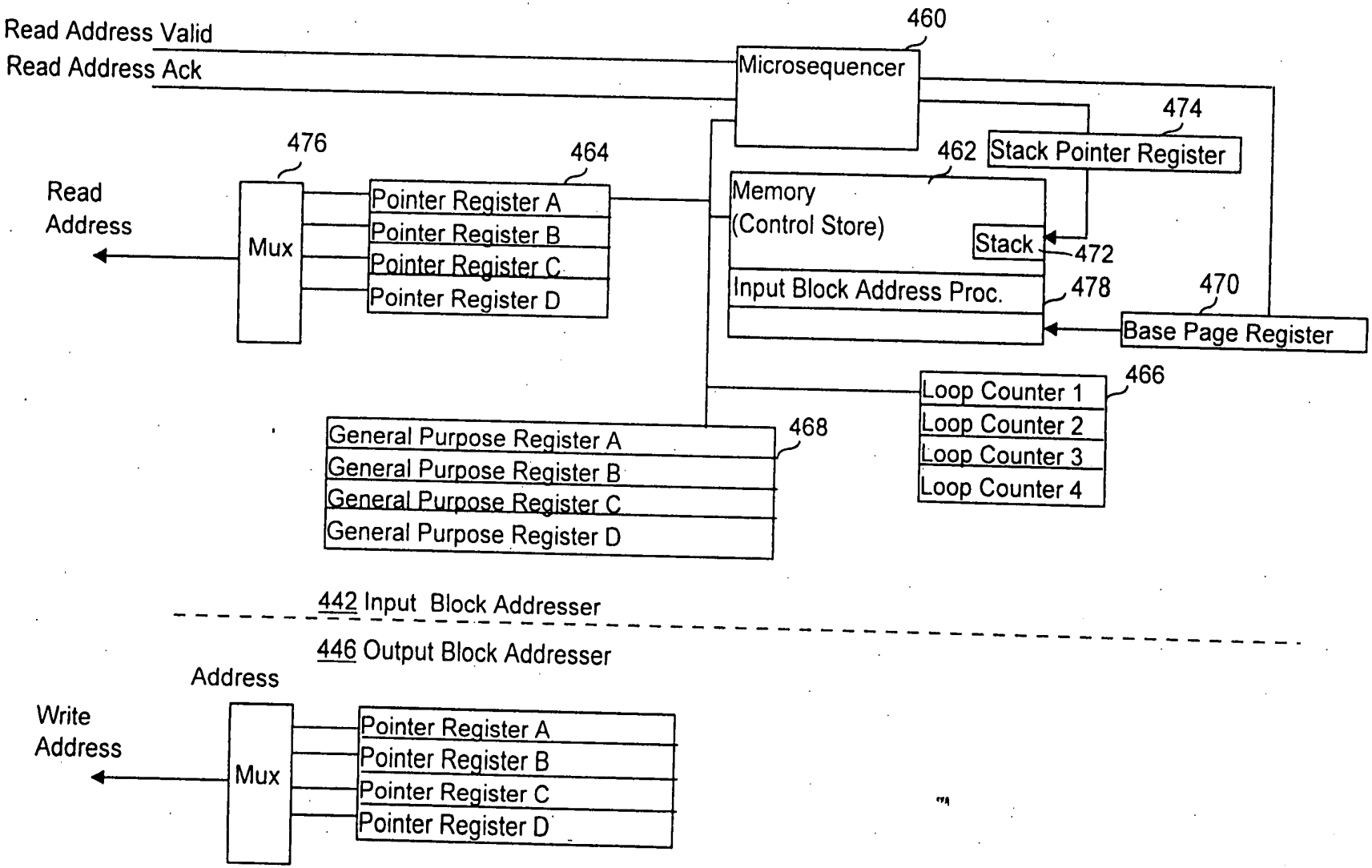

Read Address Valid
Read Address Ack
460
Microsequencer
474
Stack Pointer Register
476
464
462
Read Address
Mux
Pointer Register A
Pointer Register B
Pointer Register C
Pointer Register D
Memory (Control Store)
Stack
472
Input Block Address Proc.
478
470
Base Page Register
466
Loop Counter 1
Loop Counter 2
Loop Counter 3
Loop Counter 4
468
General Purpose Register A
General Purpose Register B
General Purpose Register C
General Purpose Register D
442 Input Block Addresser
446 Output Block Addresser
Address
Write Address
Mux
Pointer Register A
Pointer Register B
Pointer Register C
Pointer Register D

FIG. 5

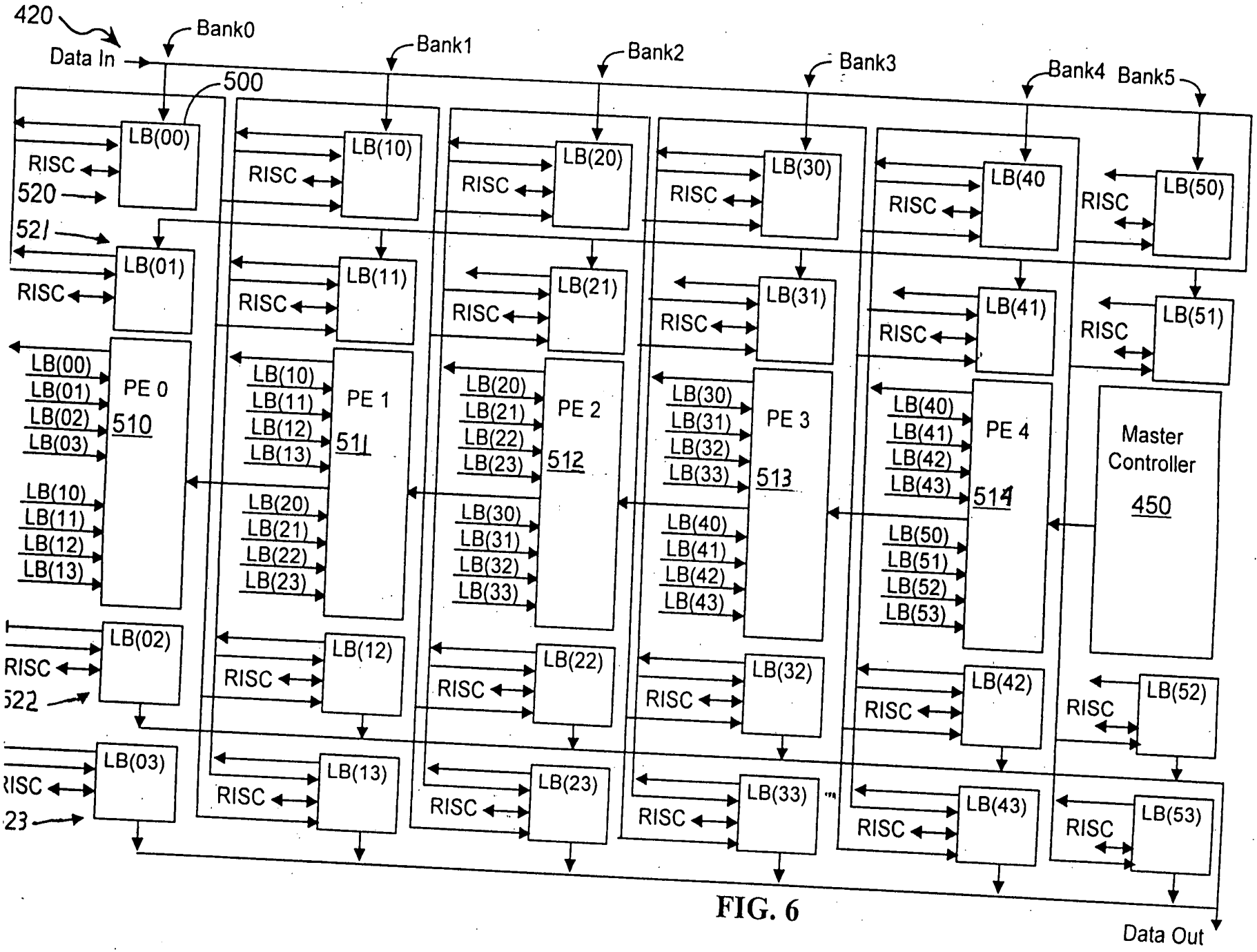


FIG. 6

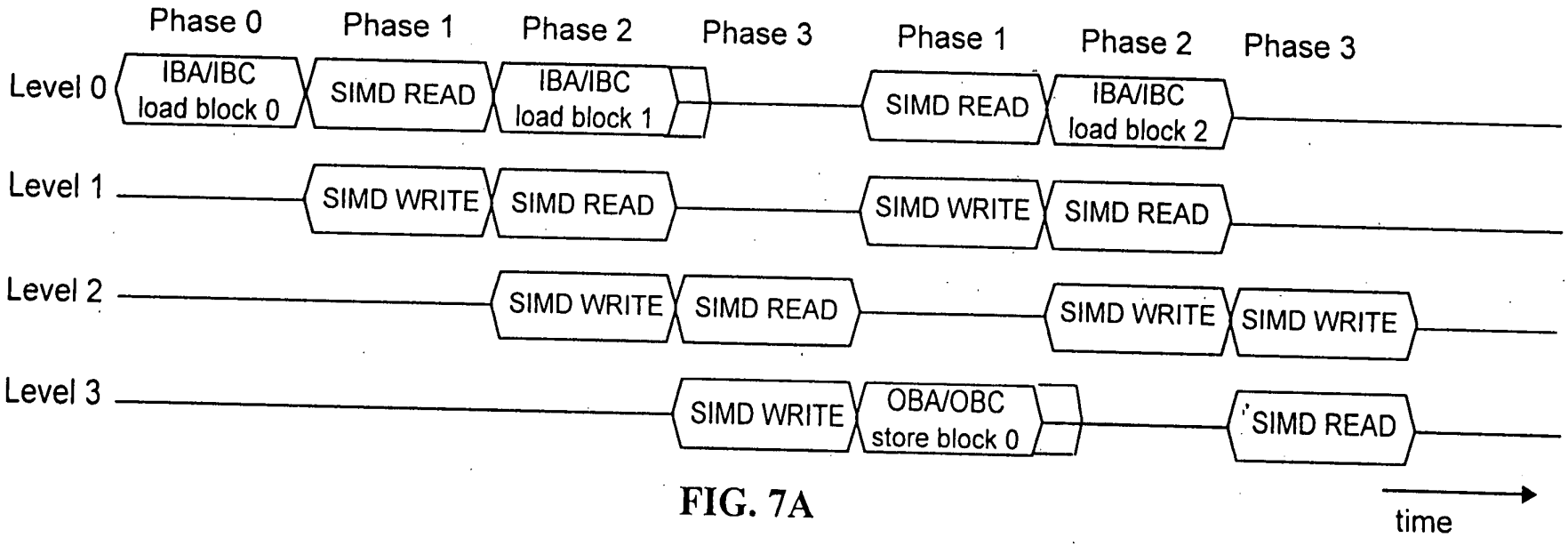


FIG. 7A

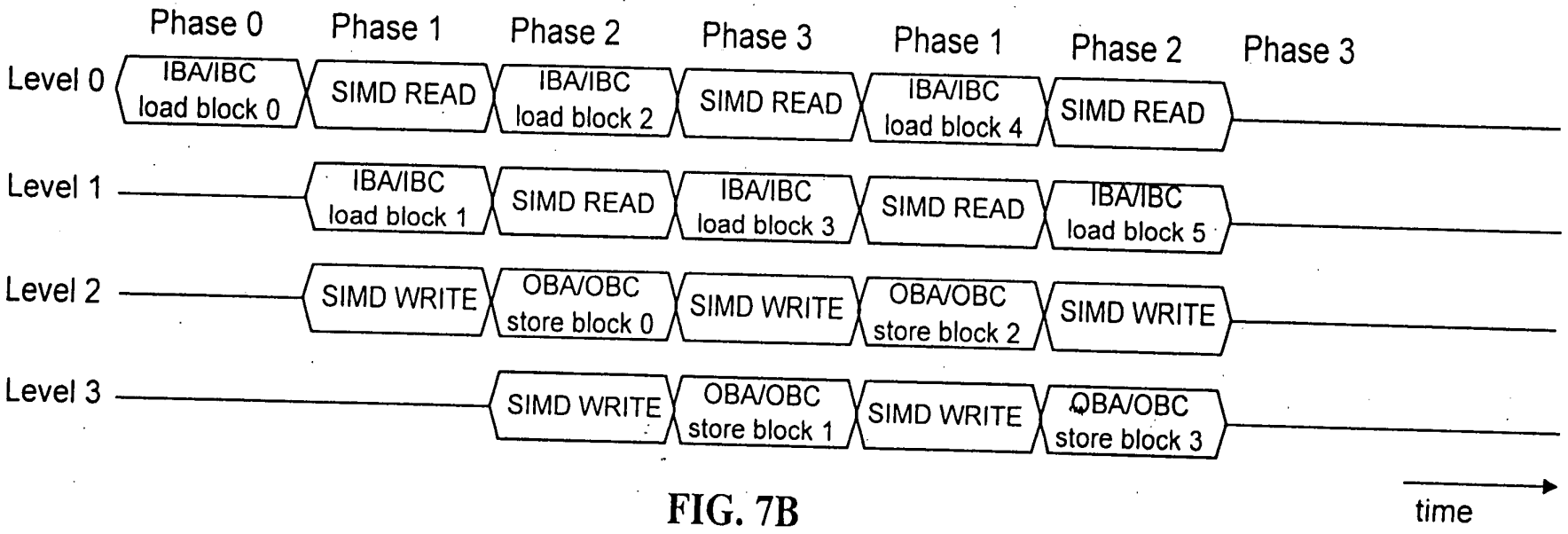


FIG. 7B

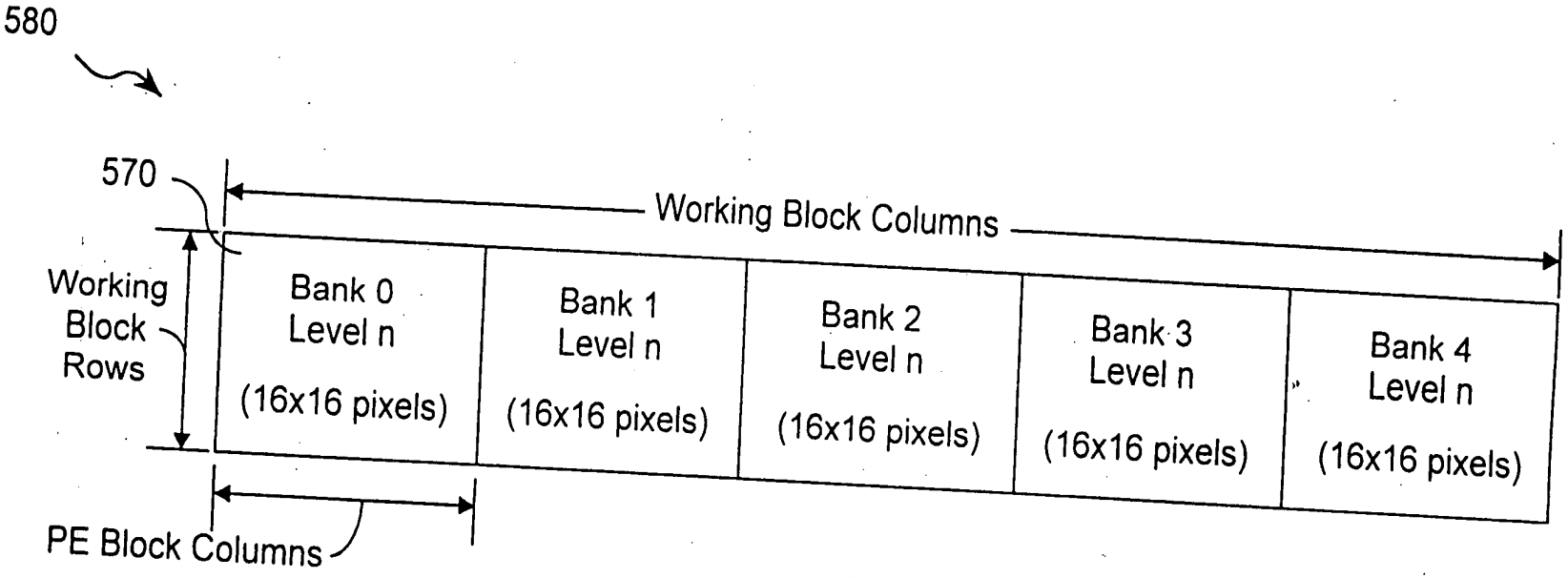
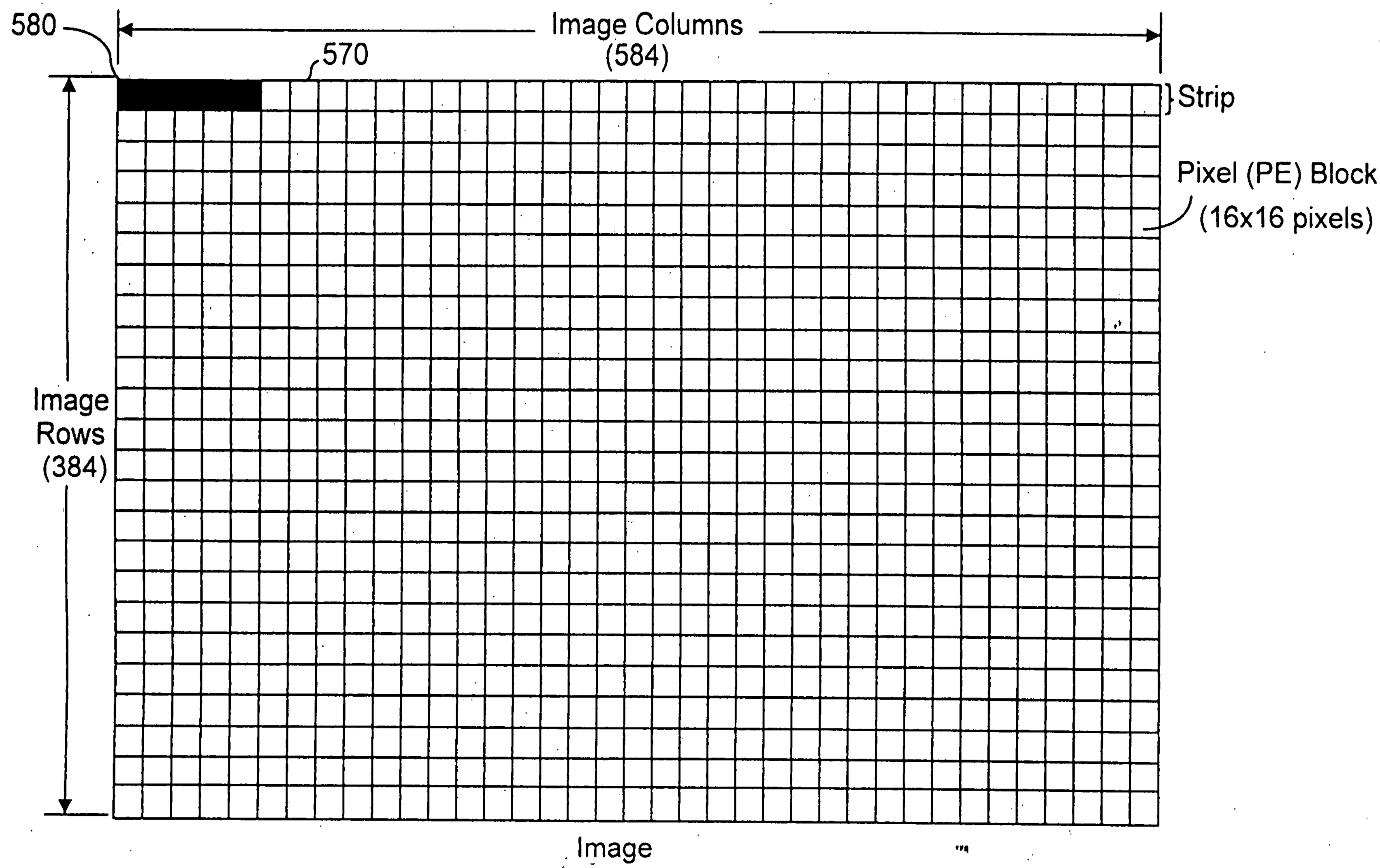
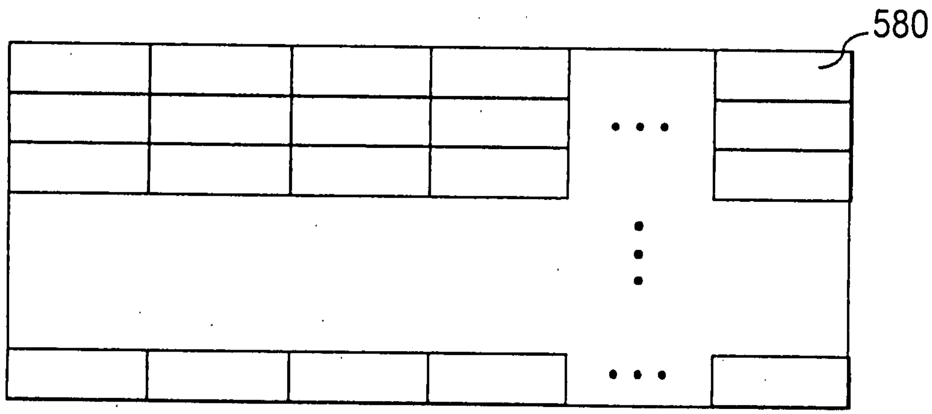


FIG. 8



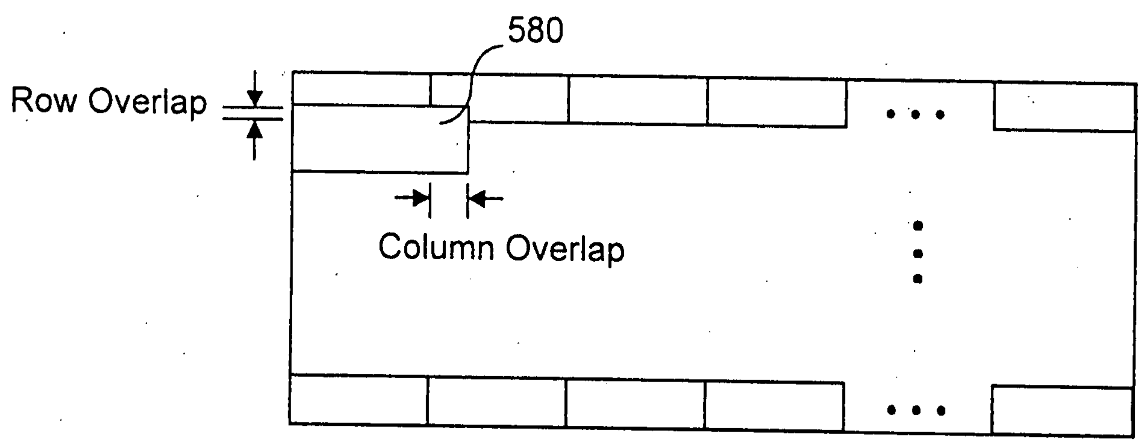
580
570
Image Columns
(584)
Strip
Pixel (PE) Block
(16x16 pixels)
Image
Rows
(384)
Image

FIG. 9



Working Blocks in Image Data

FIG. 10



Overlapping Working Blocks in Image Data

FIG. 11

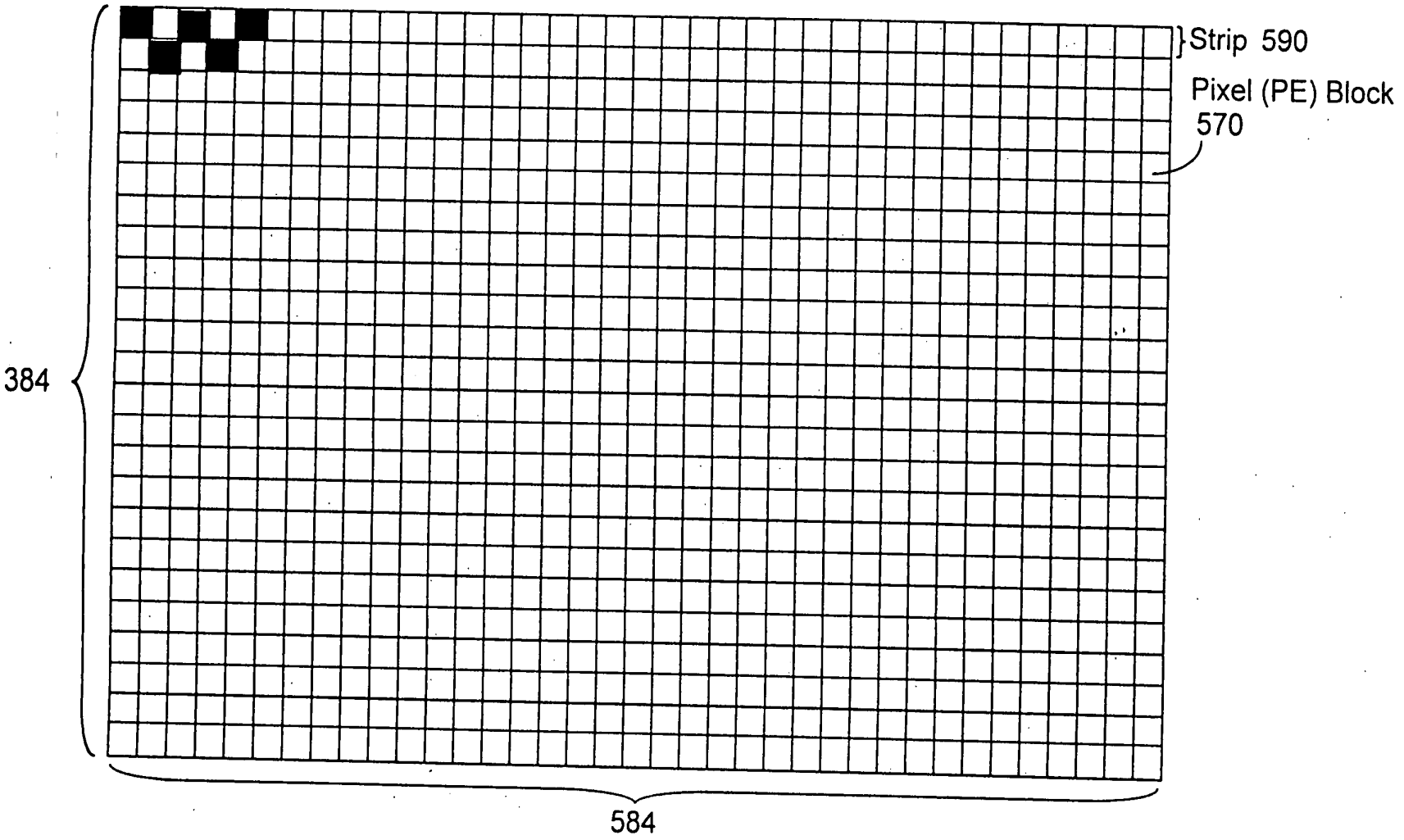


Image and Example of a dispersed processing blocks making up a working block.

FIG. 12A

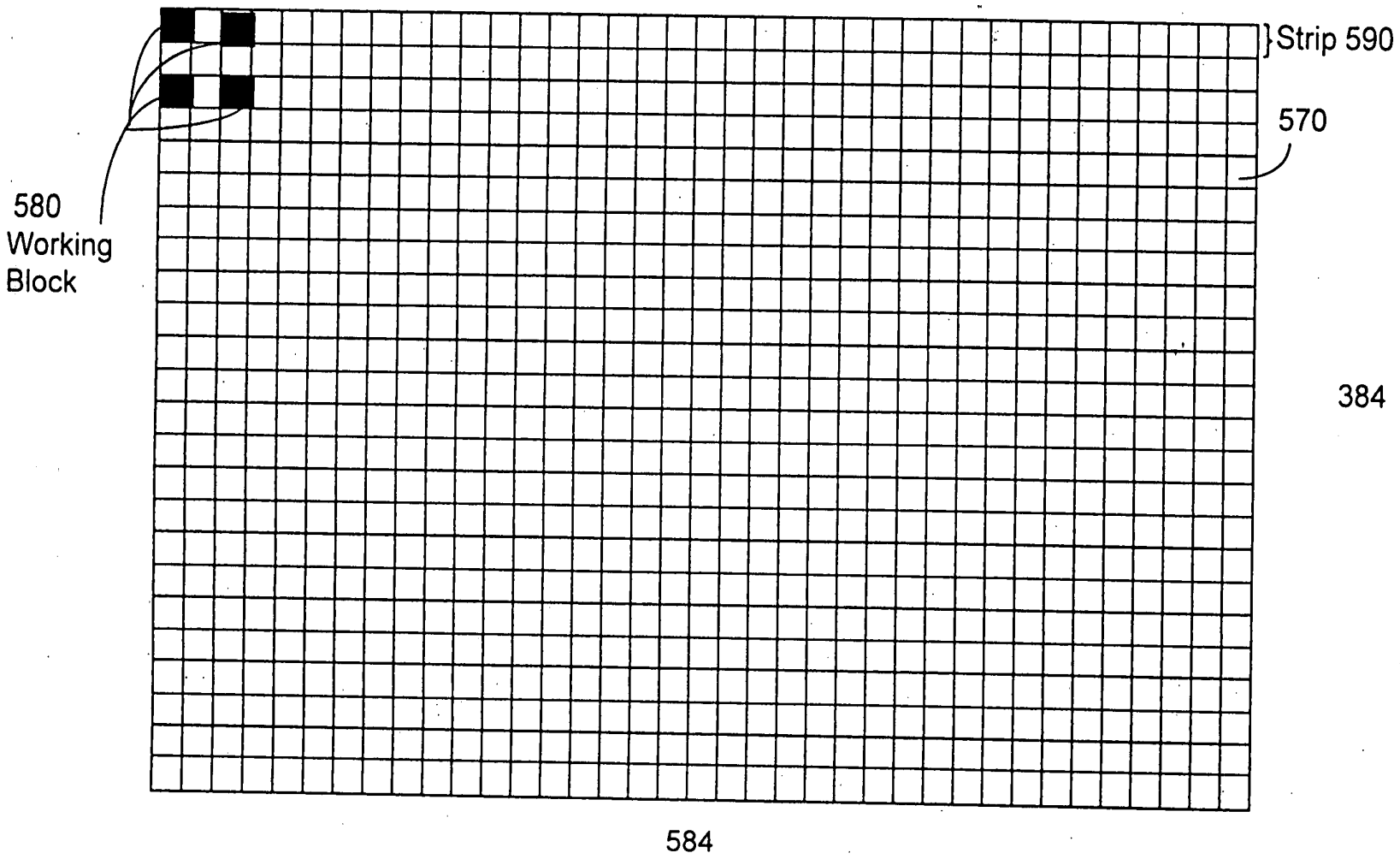


Image and Example of a dispersed processing blocks making up a working block.

FIG. 12B

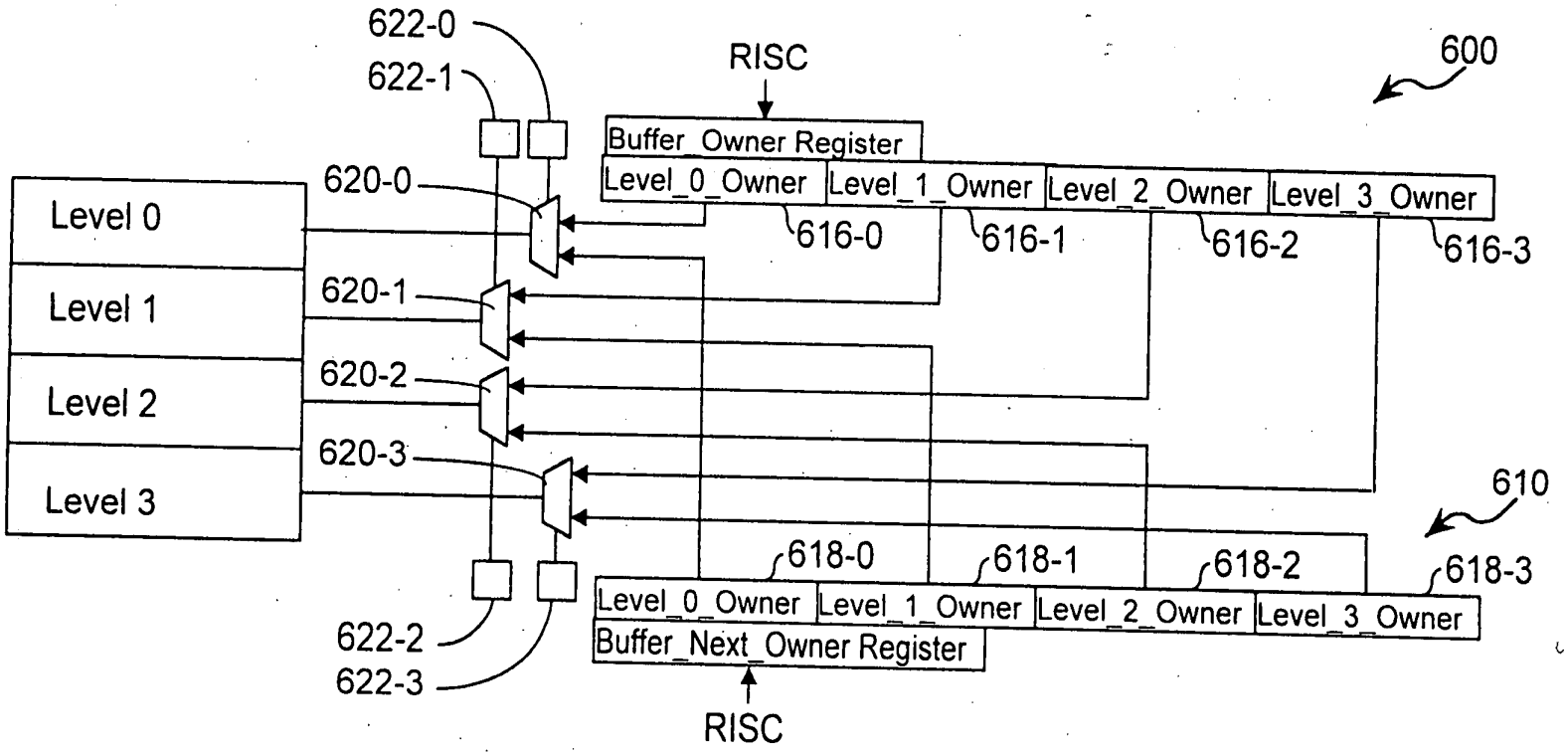

622-0
622-1
RISC
600
Buffer_Owner Register
Level_0_Owner
Level_1_Owner
Level_2_Owner
Level_3_Owner
620-0
Level 0
616-0
616-1
616-2
616-3
620-1
Level 1
620-2
Level 2
620-3
Level 3
610
618-0
618-1
618-2
618-3
Level_0_Owner
Level_1_Owner
Level_2_Owner
Level_3_Owner
622-2
622-3
Buffer_Next_Owner Register
RISC

FIG. 13

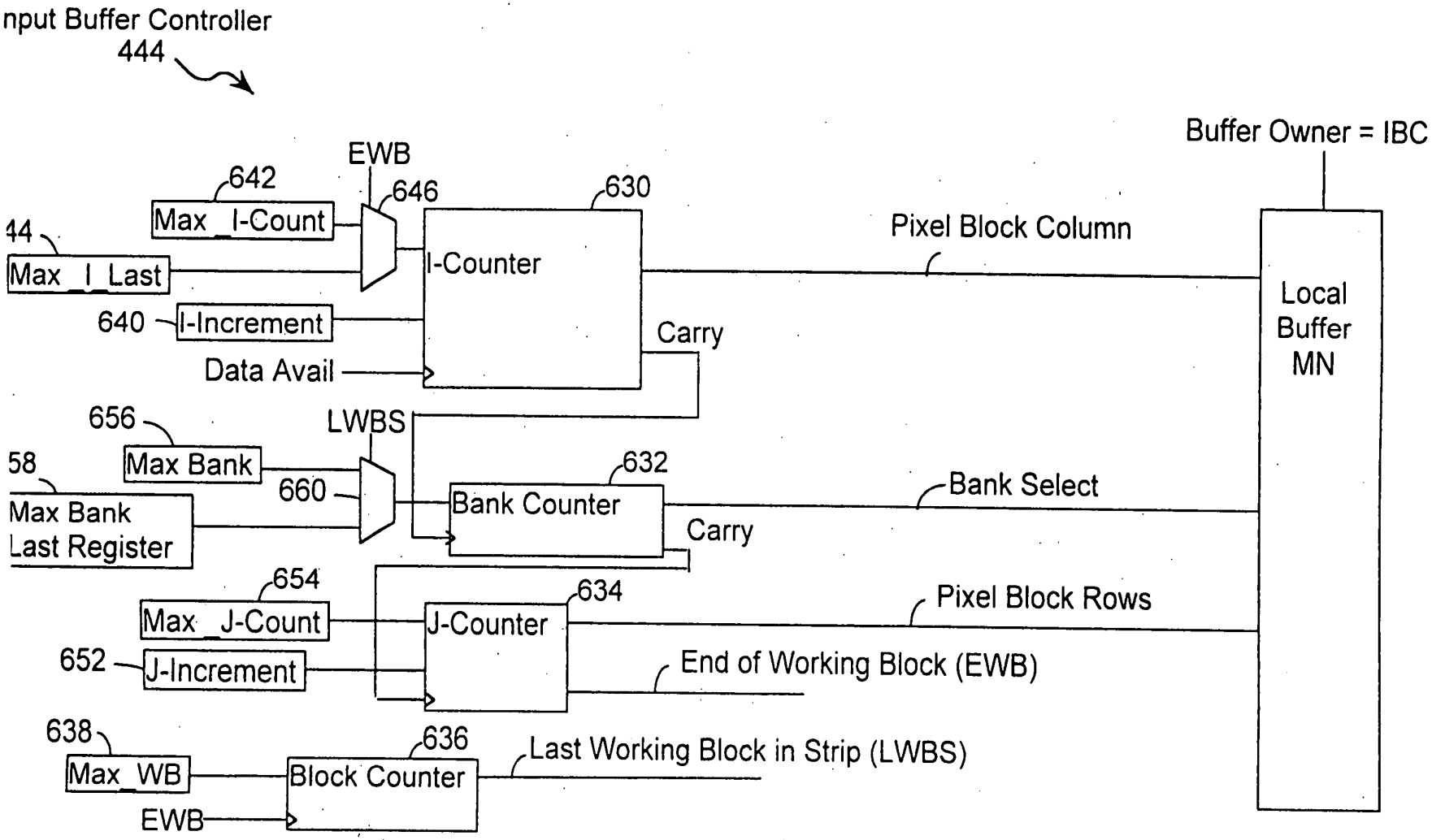
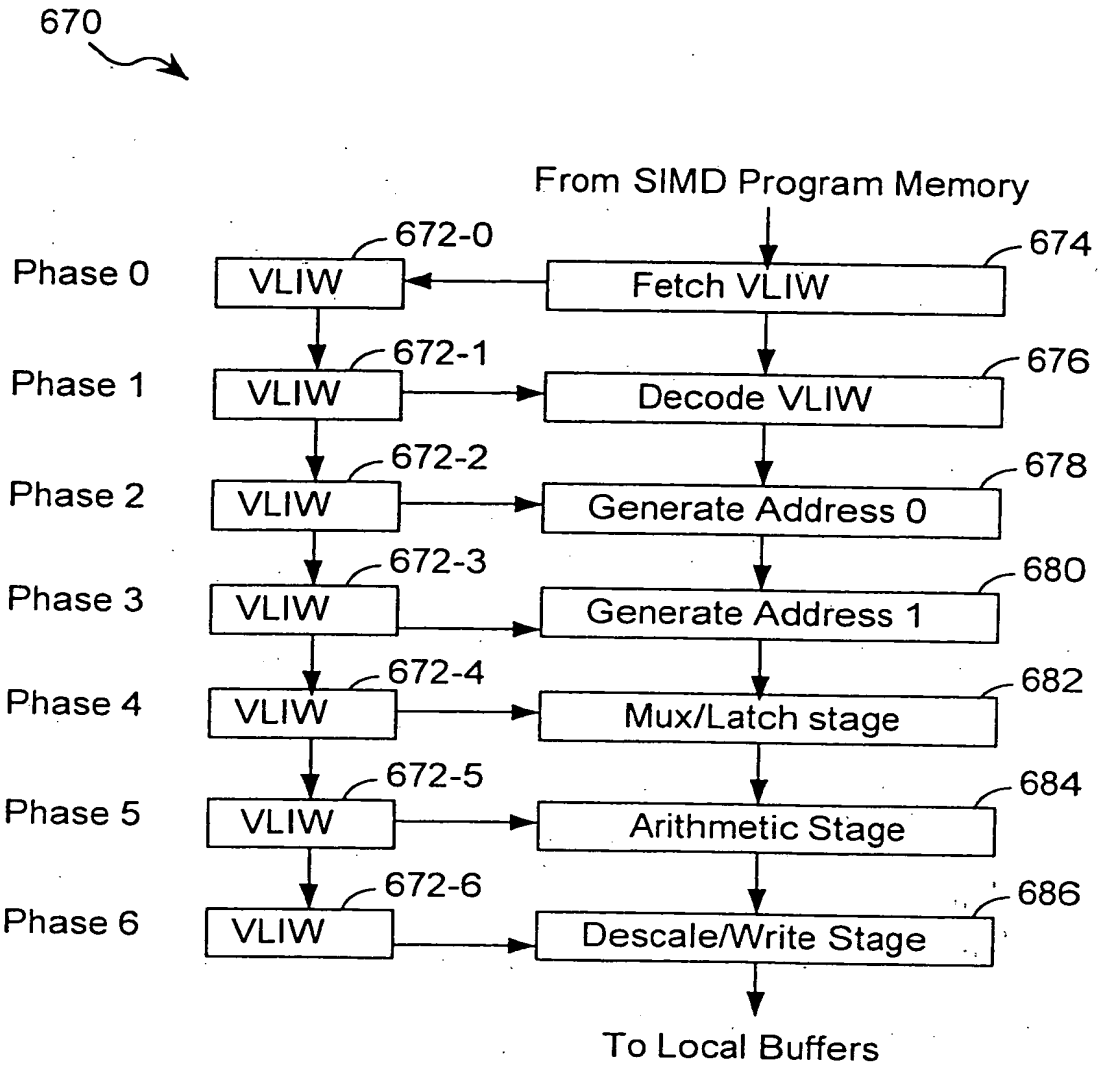

nput Buffer Controller
444
EWB
642
646
630
Max_I-Count
44
Max_I_Last
I-Counter
640
I-Increment
Data Avail
Carry
Buffer Owner = IBC
Pixel Block Column
Local Buffer MN
656
LWBS
Max Bank
58
660
632
Max Bank Last Register
Bank Counter
Bank Select
Carry
654
634
Max_J-Count
J-Counter
Pixel Block Rows
652
J-Increment
End of Working Block (EWB)
638
636
Max_WB
Block Counter
Last Working Block in Strip (LWBS)
EWB

FIG. 14



SIMD Pipeline Stages

FIG. 15

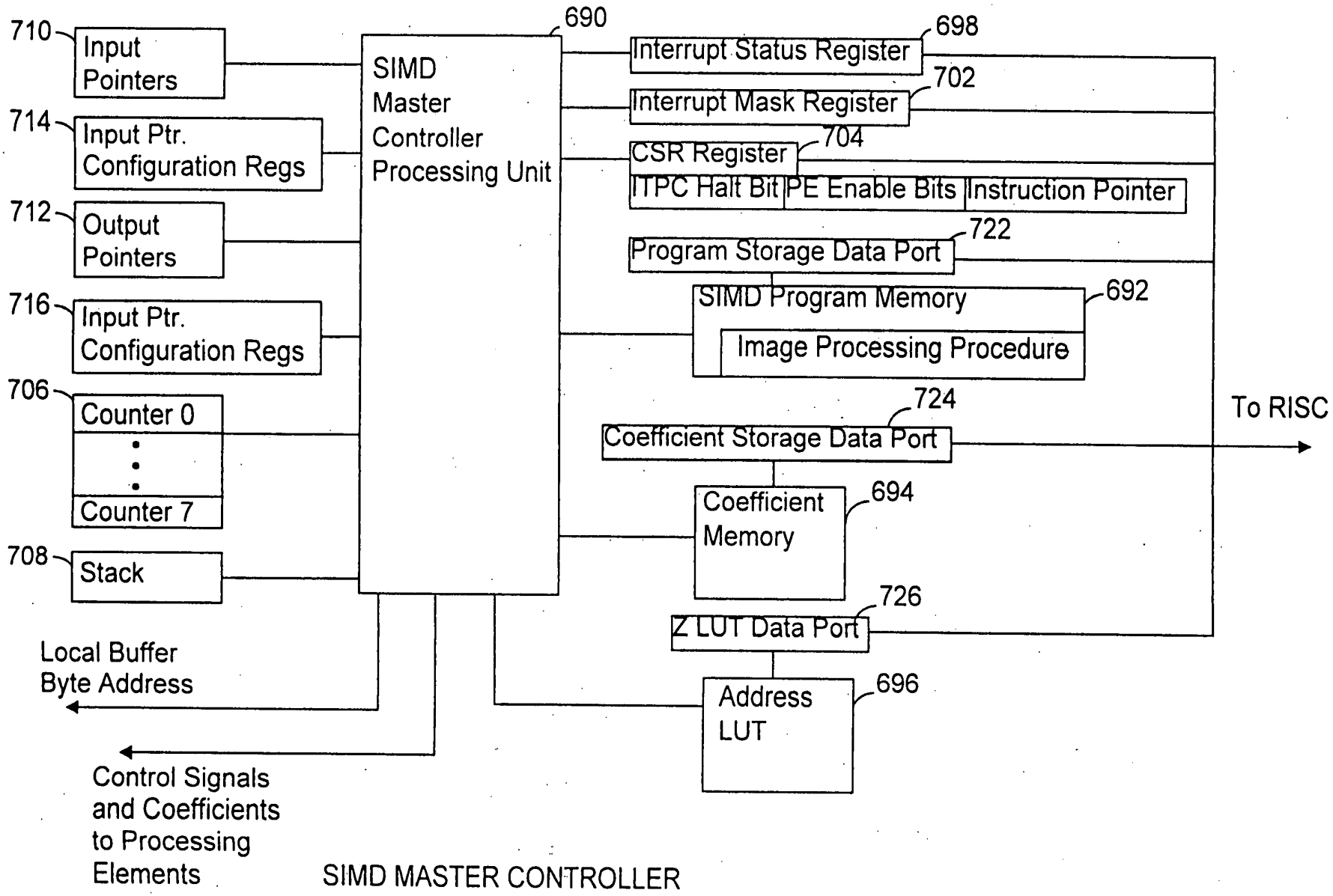
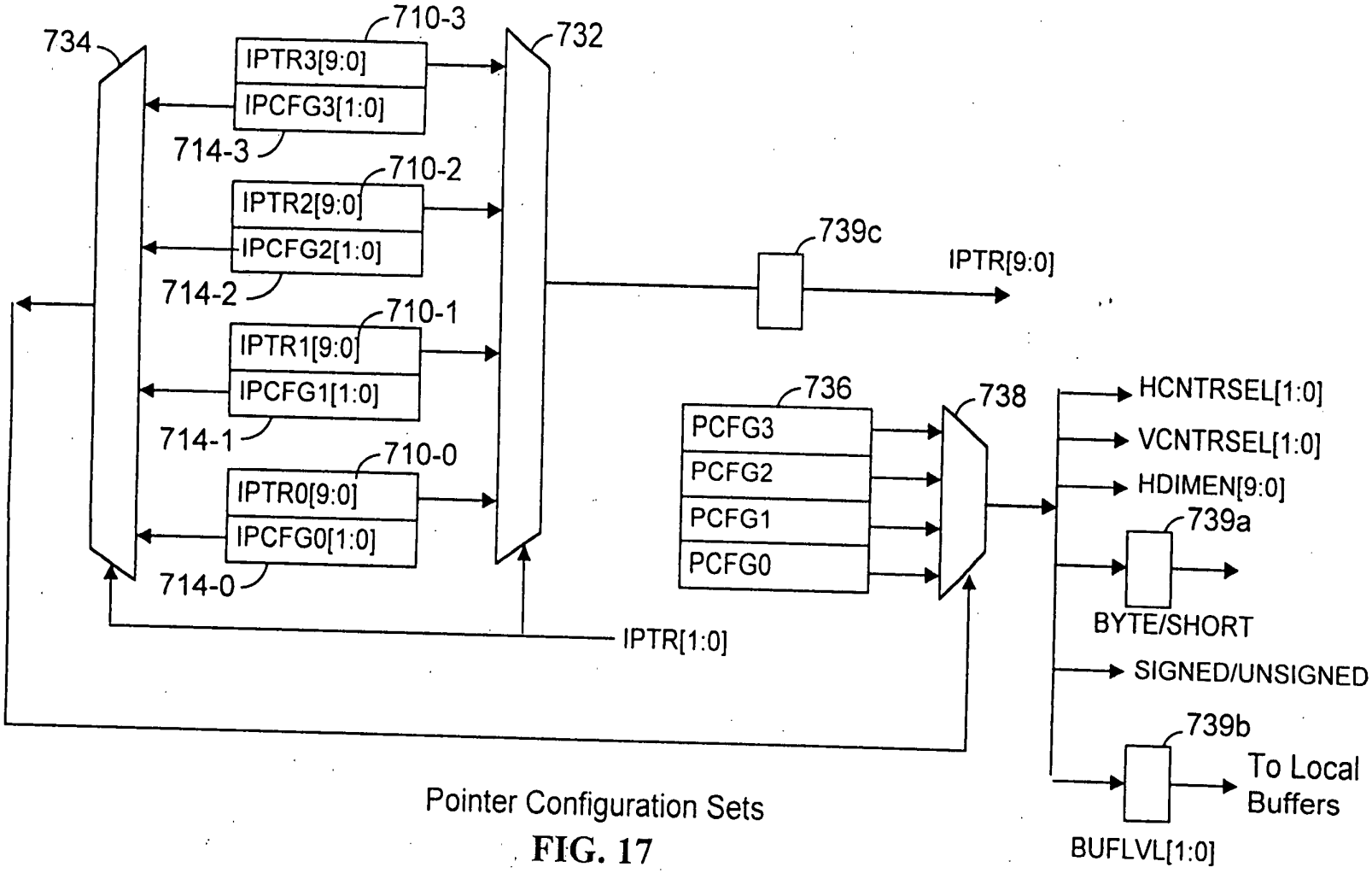
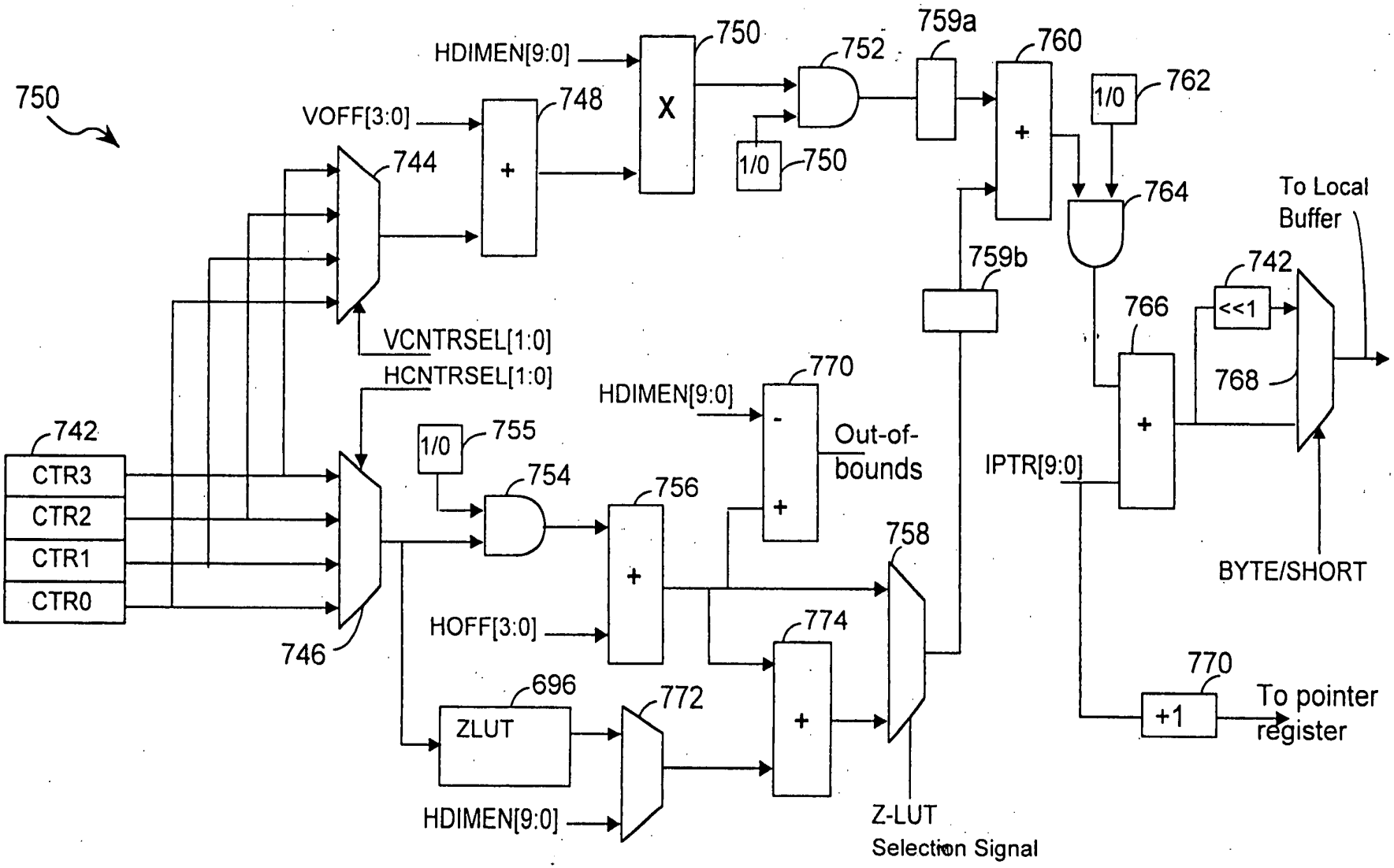

710
Input Pointers
714
Input Ptr. Configuration Regs
712
Output Pointers
716
Input Ptr. Configuration Regs
706
Counter 0
Counter 7
708
Stack
690
SIMD Master Controller Processing Unit
698
Interrupt Status Register
702
Interrupt Mask Register
704
CSR Register
ITPC Halt Bit
PE Enable Bits
Instruction Pointer
722
Program Storage Data Port
SIMD Program Memory
692
Image Processing Procedure
724
Coefficient Storage Data Port
To RISC
694
Coefficient Memory
726
Z LUT Data Port
696
Address LUT
Local Buffer Byte Address
Control Signals and Coefficients to Processing Elements
SIMD MASTER CONTROLLER

FIG. 16



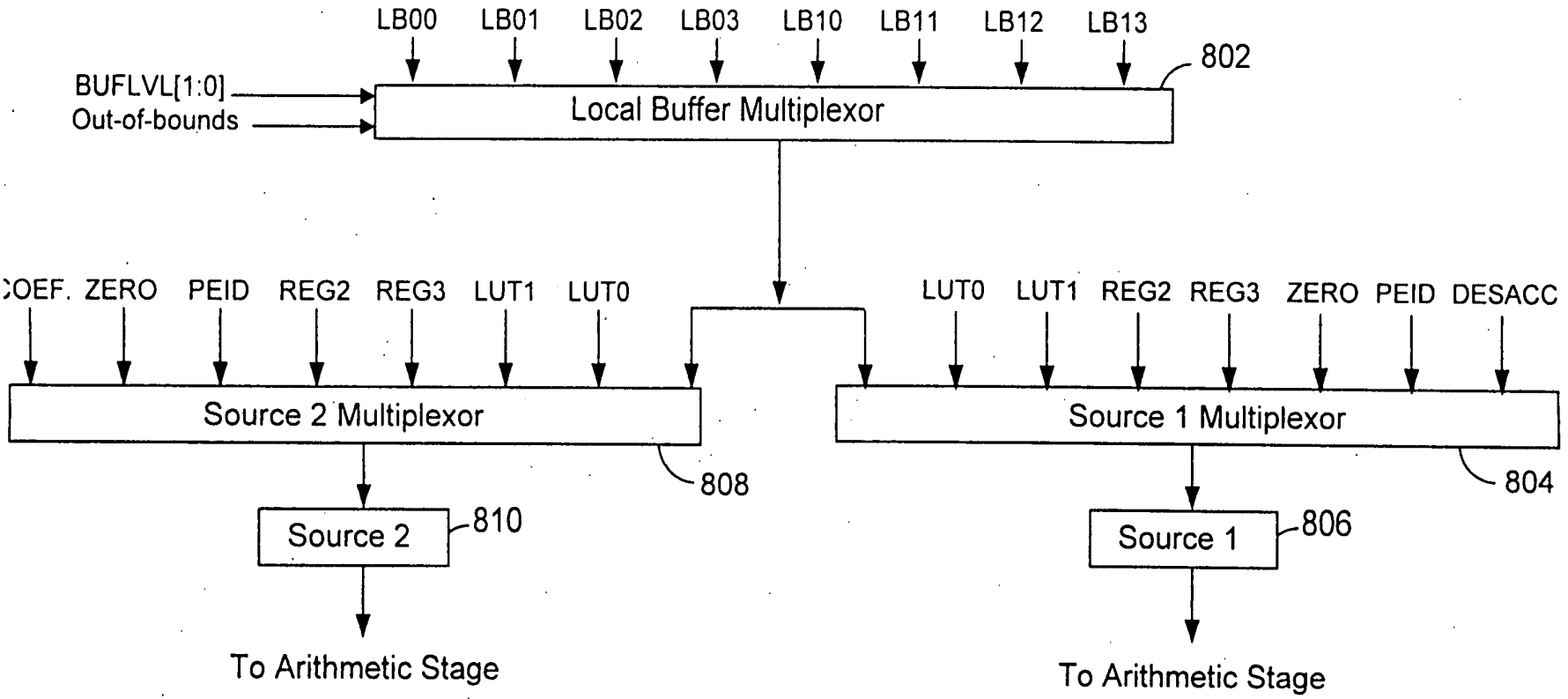
Pointer Configuration Sets

FIG. 17



EFFECTIVE ADDRESS GENERATION

FIG. 18



Processing Element
Multiplexor/Latch Stage

FIG. 19

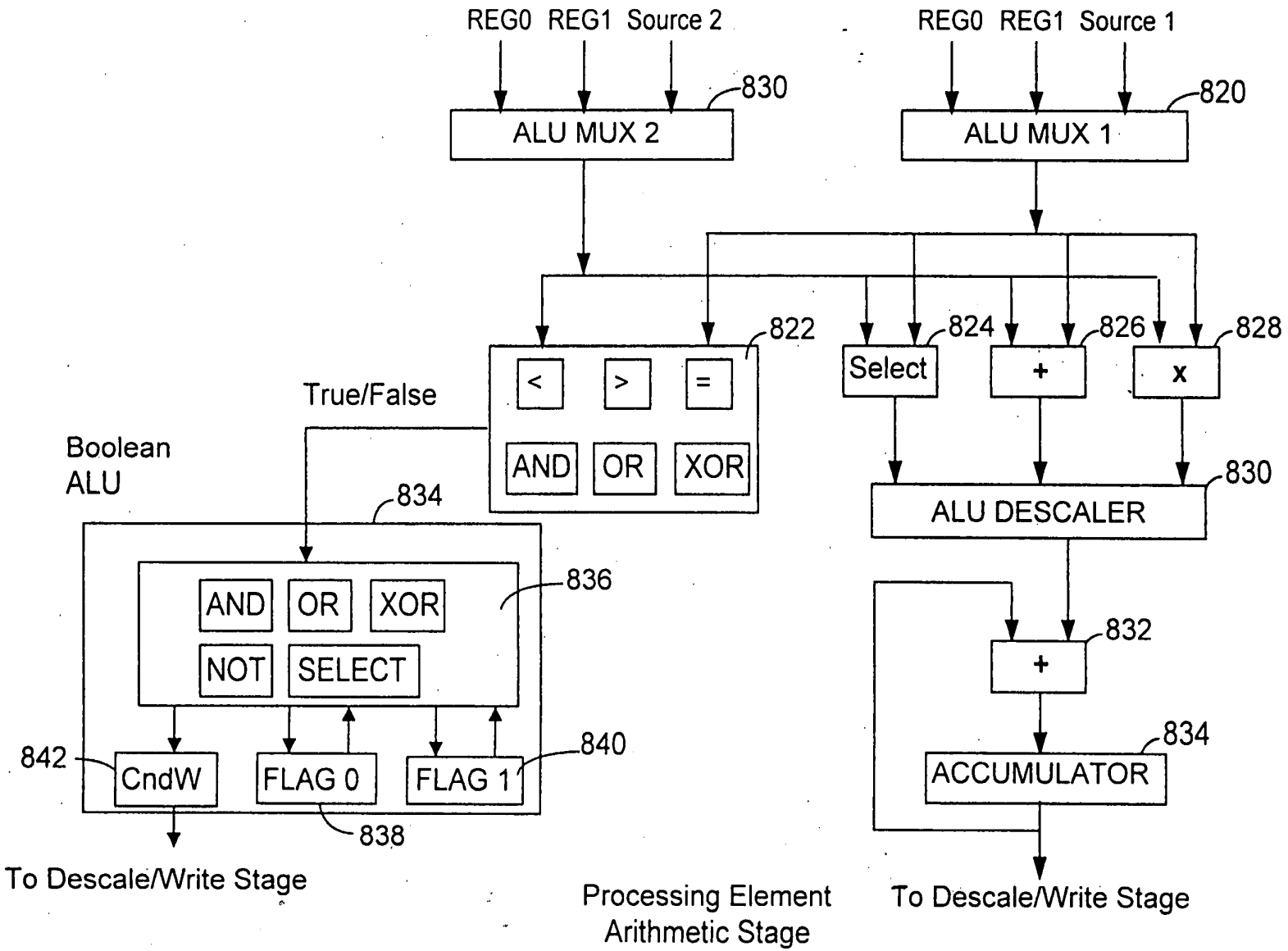
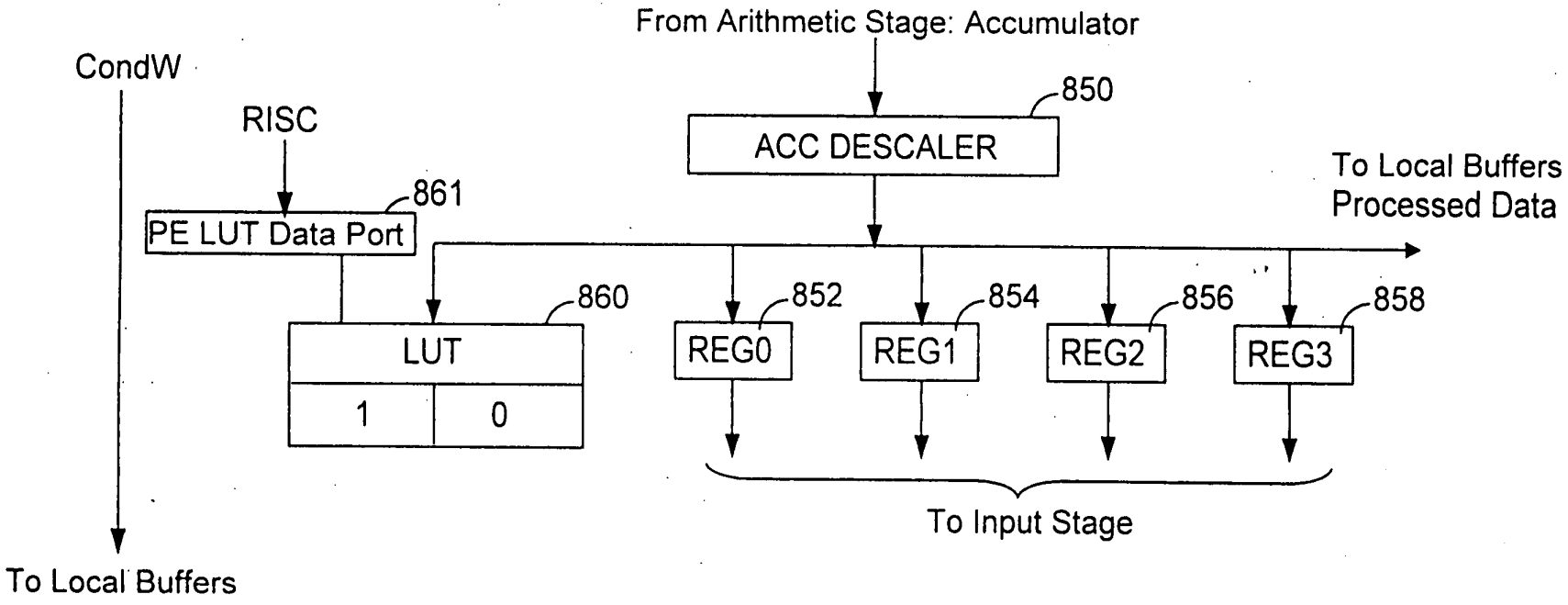

REG0 REG1 Source 2
REG0 REG1 Source 1
830
820
ALU MUX 2
ALU MUX 1
822
824
826
828
<
>
=
Select
+
x
True/False
Boolean
ALU
AND
OR
XOR
834
830
ALU DESCALER
AND
OR
XOR
836
NOT
SELECT
832
+
842
CndW
FLAG 0
FLAG 1
840
834
ACCUMULATOR
838
To Descale/Write Stage
Processing Element
Arithmetic Stage
To Descale/Write Stage

FIG. 20



Processing Element
Descale/Write Stage

FIG. 21

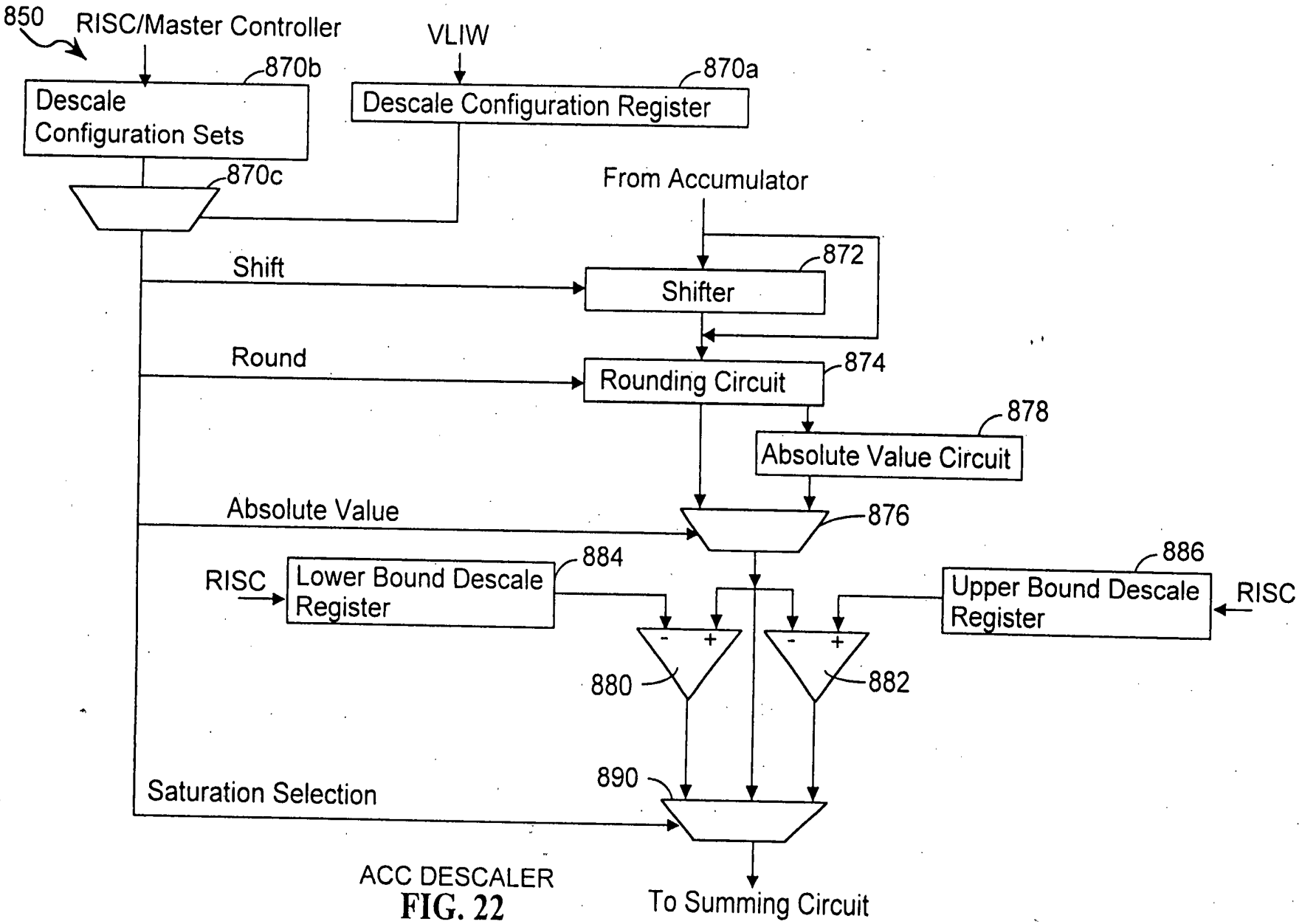

850
RISC/Master Controller
VLIW
870b
Descale Configuration Sets
870a
Descale Configuration Register
870c
From Accumulator
Shift
872
Shifter
Round
Rounding Circuit
874
878
Absolute Value Circuit
Absolute Value
876
884
RISC
Lower Bound Descale Register
886
Upper Bound Descale Register
RISC
-
+
880
882
890
Saturation Selection
ACC DESCALER
To Summing Circuit

FIG. 22

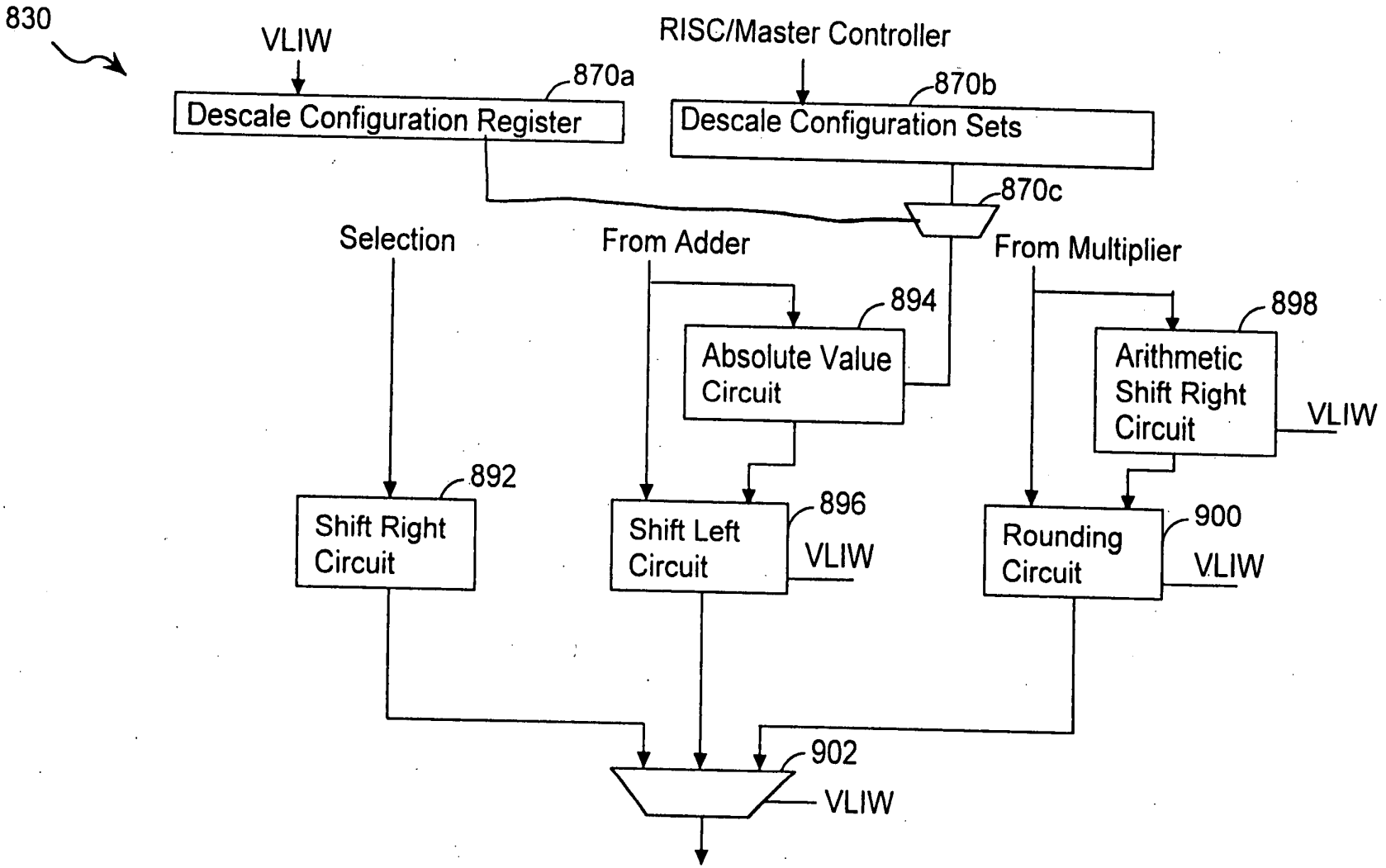

830
VLIW
RISC/Master Controller
870a
Descale Configuration Register
870b
Descale Configuration Sets
870c
Selection
From Adder
From Multiplier
894
Absolute Value Circuit
898
Arithmetic Shift Right Circuit
VLIW
892
Shift Right Circuit
896
Shift Left Circuit
VLIW
900
Rounding Circuit
VLIW
902
VLIW
To Accumulator
ALU DESCALER

FIG. 23

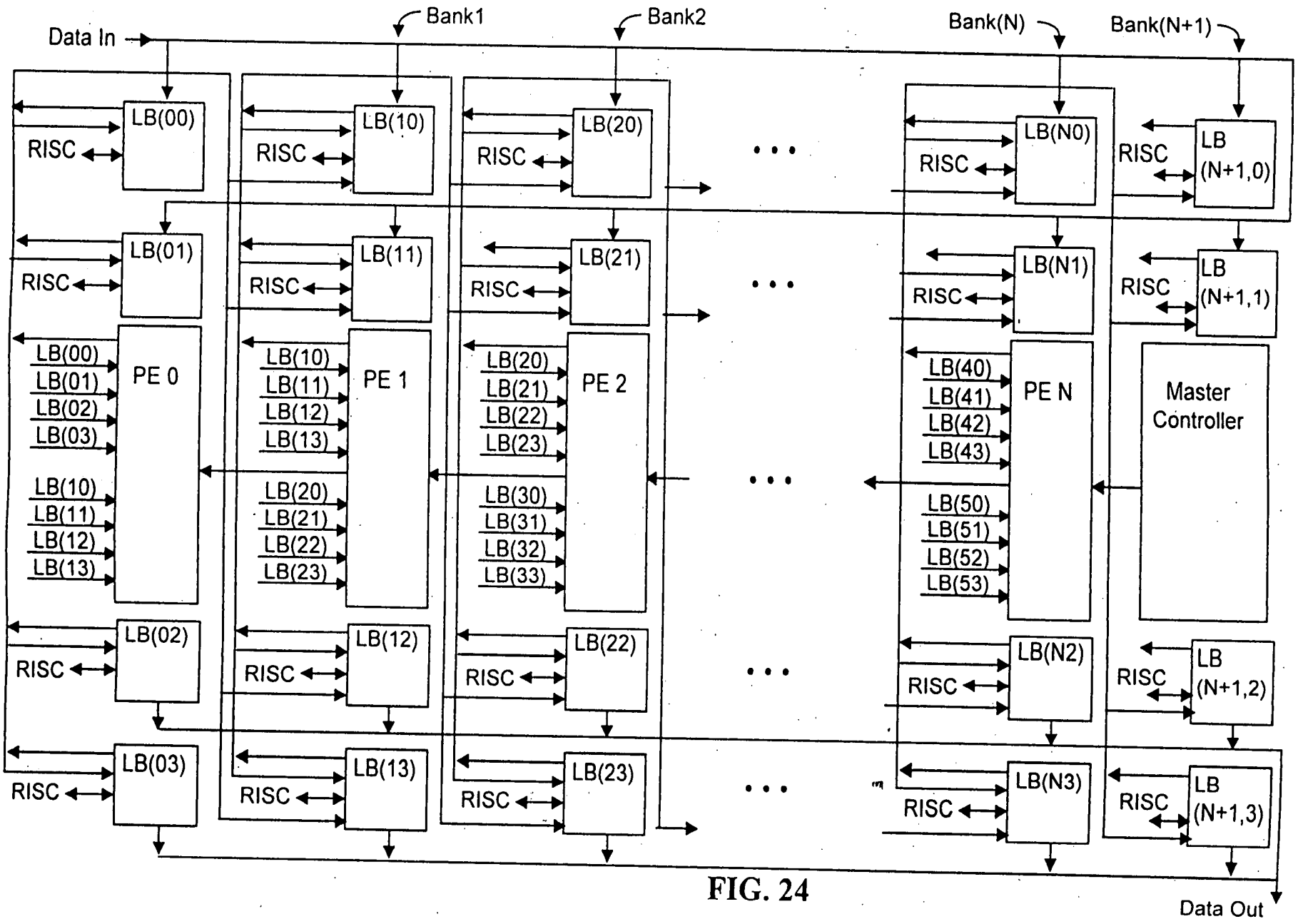


FIG. 24

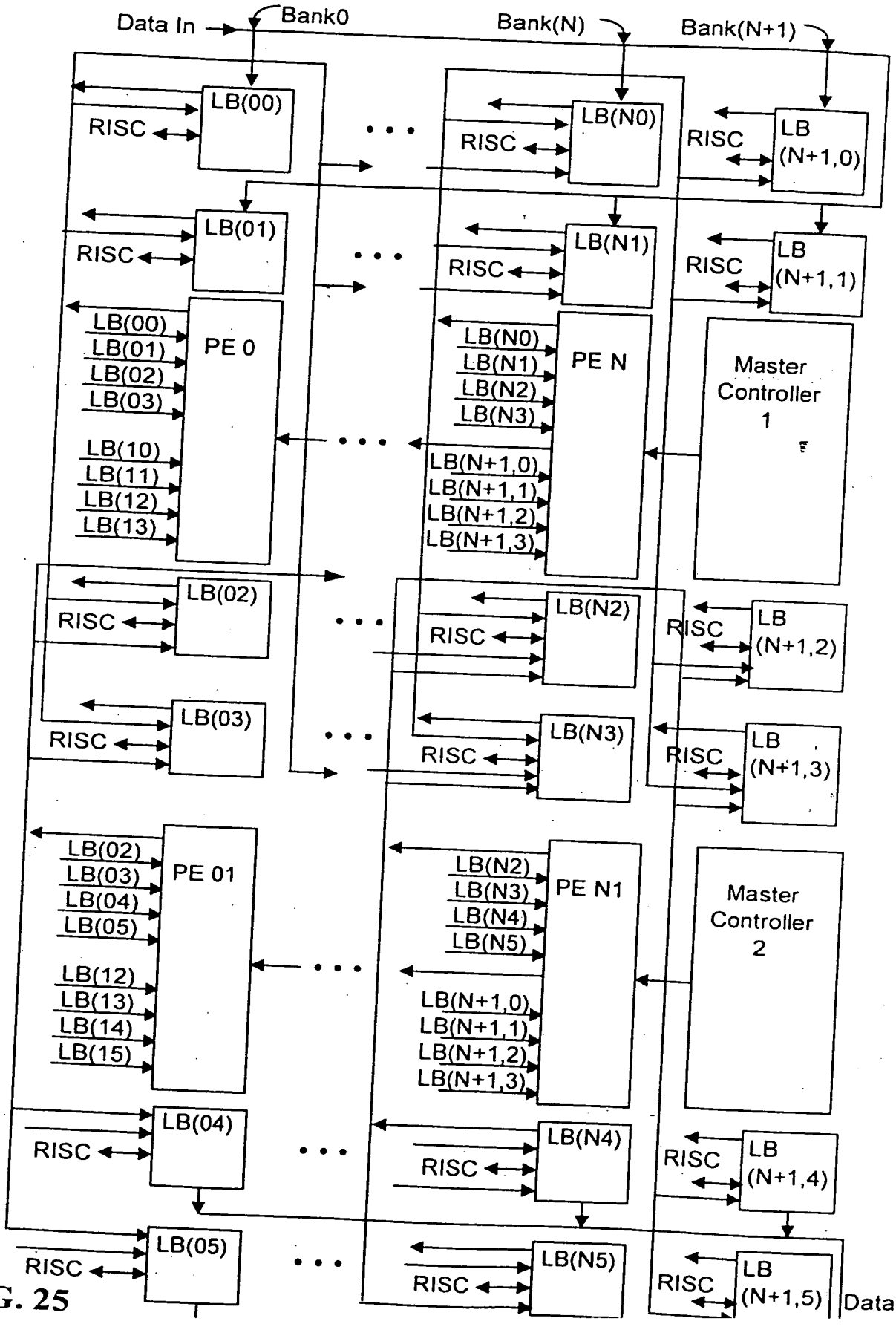

Data In
Bank0
Bank(N)
Bank(N+1)
LB(00)
RISC
LB(N0)
LB (N+1,0)
LB(01)
LB(N1)
LB (N+1,1)
PE 0
LB(00)
LB(01)
LB(02)
LB(03)
LB(10)
LB(11)
LB(12)
LB(13)
PE N
LB(N0)
LB(N1)
LB(N2)
LB(N3)
LB(N+1,0)
LB(N+1,1)
LB(N+1,2)
LB(N+1,3)
Master Controller 1
LB(02)
LB(N2)
LB (N+1,2)
LB(03)
LB(N3)
LB (N+1,3)
PE 01
LB(02)
LB(03)
LB(04)
LB(05)
LB(12)
LB(13)
LB(14)
LB(15)
PE N1
LB(N2)
LB(N3)
LB(N4)
LB(N5)
LB(N+1,0)
LB(N+1,1)
LB(N+1,2)
LB(N+1,3)
Master Controller 2
LB(04)
LB(N4)
LB (N+1,4)
LB(05)
LB(N5)
LB (N+1,5)
Data

FIG. 25

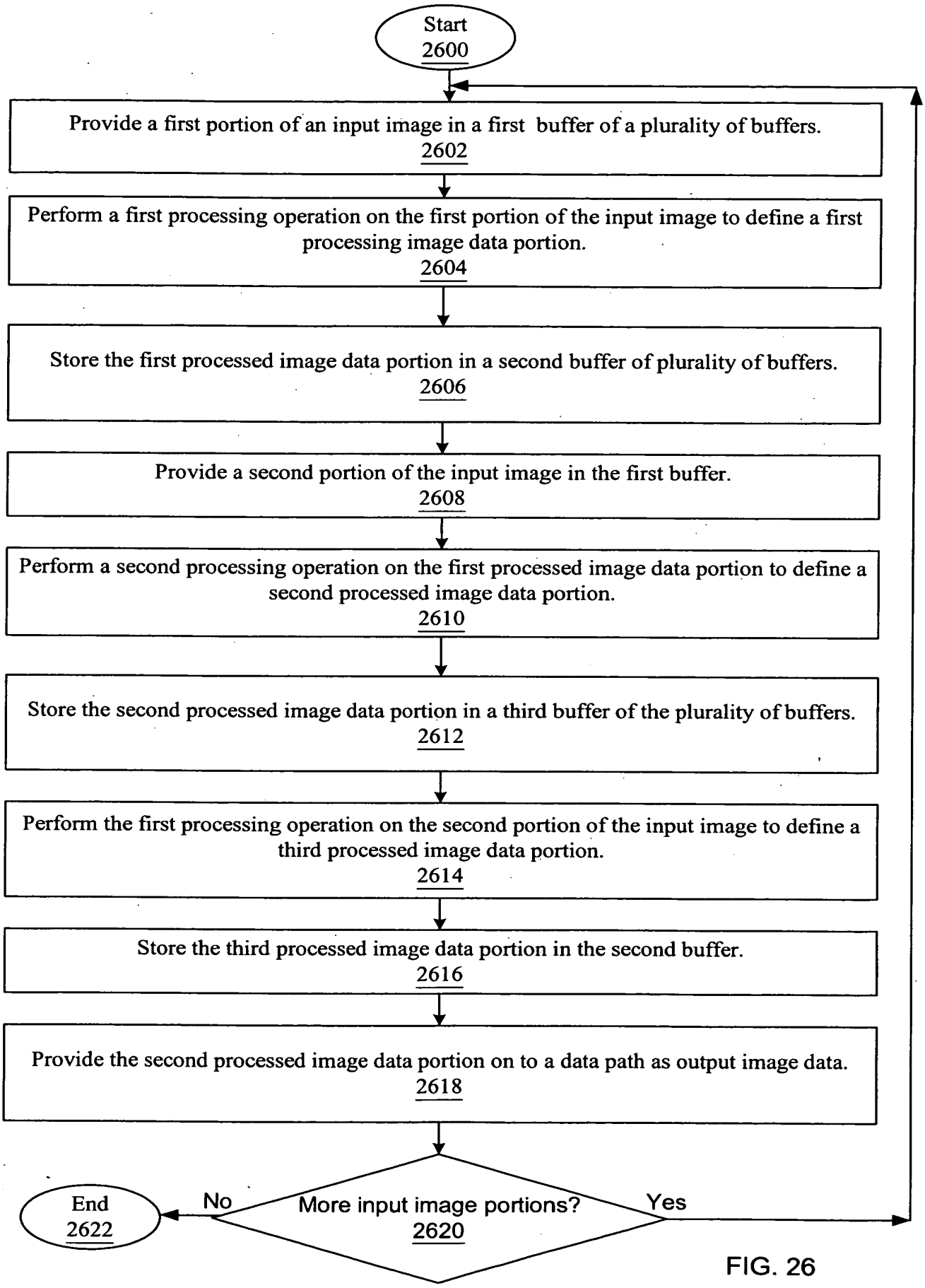

Start
2600
Provide a first portion of an input image in a first buffer of a plurality of buffers.
2602
Perform a first processing operation on the first portion of the input image to define a first processing image data portion.
2604
Store the first processed image data portion in a second buffer of plurality of buffers.
2606
Provide a second portion of the input image in the first buffer.
2608
Perform a second processing operation on the first processed image data portion to define a second processed image data portion.
2610
Store the second processed image data portion in a third buffer of the plurality of buffers.
2612
Perform the first processing operation on the second portion of the input image to define a third processed image data portion.
2614
Store the third processed image data portion in the second buffer.
2616
Provide the second processed image data portion on to a data path as output image data.
2618
More input image portions?
2620
No
Yes
End
2622

FIG. 26